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FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE				ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,7433		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 22, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
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2 of 27							



CHAPTER 200: Clinical presentation and management of patients with non-communicable diseases

3 of 27



FORM PTO 1449 MODIFIED
U.S. PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
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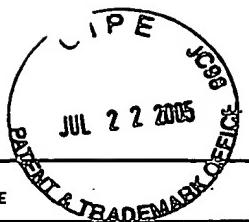
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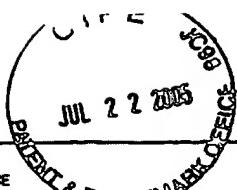
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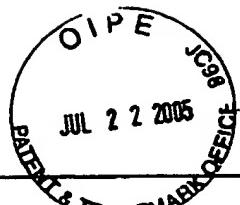
8 of 27



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9 of 27





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12 of 27



FORM PTO 1449 MODIFIED
U.S. PATENT AND TRADEMARK OFFICE

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APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
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13 of 27

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JUL 22 2005
JC88
PATENT & TRADEMARK OFFICE

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
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LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
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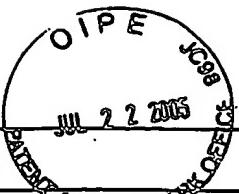
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14 of 27



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APPLICANT

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FILING DATE	GROUP
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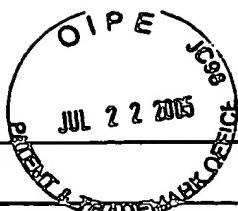
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16 of 27



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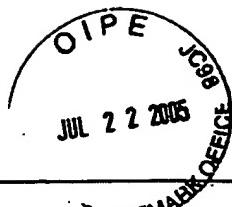
17 of 27



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18 of 27



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19 of 27



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				MP0020	09/737,743		
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20 of 27



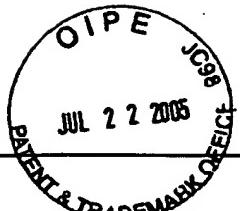
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		Sehat SUTARDJA					
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21 of 27



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22 of 27



FORM PTO 1449 MODIFIED
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

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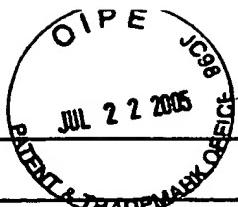
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23 of 27



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24 of 27



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25 of 27

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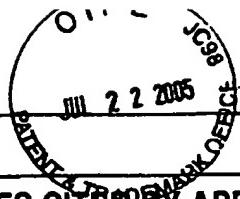
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26 of 27





FORM PTO 1449 MODIFIED
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
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FILING DATE	GROUP
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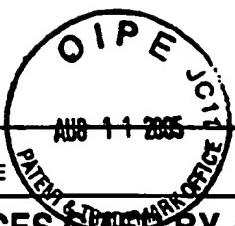
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<i>✓</i>	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm ²			
EXAMINER	<i>pmlm</i>	DATE CONSIDERED		<i>9/13/05</i>
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ATTORNEY DOCKET NO.

APPLICATION NO.

MP0020

09/737.743

APPLICANT

Sehat SUTARDJA

LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: August 11, 2005

100-PATENT DOCUMENTS

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12/18/2000

2631

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		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
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*EXAMINER INITIALS			
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